CLAIMS

1. A method for providing a horizontal scan control signal (S_{LS}) for a TV set from a horizontal synchronization signal (S_{HS}) contained in a composite video signal (CVBS), the horizontal synchronization signal (S_{HS}) containing horizontal synchronization pulses (39) and parasitic pulses (40), said scan control signal (S_{LS}) being provided from an oscillating signal (S_O) generated by an oscillator (26) of a phase-locked loop (20) receiving the horizontal synchronization signal (S_{HS}), said oscillating signal (S_O) having a frequency depending on a driving signal (S_C) provided from the comparison between the horizontal synchronization signal (S_{HS}) and a binary phase signal (PH, PH'), wherein, at each parasitic pulse (39) among successive parasitic pulses between two synchronization pulses (40), the driving signal (S_C) is successively varied in the increasing direction or in the decreasing direction.

2. The method of claim 1, wherein the parasitic pulses have variable durations.

3. A circuit for providing a horizontal scan control signal (S_{LS}) for a TV set from a horizontal synchronization signal (S_{HS}) contained in the composite video signal (CVBS), the horizontal synchronization signal (S_{HS}) containing horizontal synchronization pulses (39) and parasitic pulses (40), said circuit comprising a phase-locked loop (20) receiving the horizontal synchronization signal (S_{HS}) comprising an oscillator (26) generating an oscillating signal (S_O) from which is provided the scan control signal (S_{LS}), the frequency of the oscillating circuit (S_O) depending on a driving signal (S_C) provided from the horizontal synchronization signal (S_{HS}), and comprising a means (50, 22, 24) for correcting the driving signal (S_C) which, at each parasitic pulse (40) among successive parasitic pulses between two synchronization pulses (39), alternately varies the driving signal (S_C) in the increasing or decreasing direction.

4. The method of claim 3, further comprising:

a comparator (22) for comparing the horizontal synchronization signal (S_{HS}) and a modified phase signal (PH') and providing, according to the comparison, a current (I_{PLL}) of zero amplitude or of constant amplitude and of variable sign;

a capacitor (24) run through by the current (I_{PLL}) and providing the driving signal (S_C); and

a correction circuit (50) providing the comparator (24) with the modified phase signal (PH') corresponding to a binary phase signal (PH) having a frequency proportional to the frequency of the oscillating signal (S_O) or corresponding to a binary correction signal (S_Q), the state of which switches for each parasitic pulse (40).

5. The circuit of claim 4, wherein the correction circuit (50) comprises a switch (55) adapted to alternately connecting, according to a switch control signal (S_{IC}), an output terminal (52) connected to the comparator (22) at a first input terminal (51) receiving the phase signal (PH) or at a second input terminal receiving the correction signal (S_Q), the switch signal (S_{IC}) being provided from a binary signal at a first state at the level of a synchronization pulse (39) and at a second state otherwise.

6. The circuit of claim 5, wherein the switch signal (S_{IC}) is also provided from at least one binary validation signal (S_M, S_{STAND}, S_{PLLV}) at a first state when a validation condition is fulfilled and at a second state when the validation condition is not fulfilled.

7. The circuit of claim 4, comprising a latch (54) providing the correction signal (S_Q) receiving a binary latch control signal (S_{LC}) provided from the horizontal synchronization signal (S_{HS}), the state of the correction signal (S_Q) switching at each falling edge of the latch control signal (S_{LC}).

8. The circuit of claim 7, comprising a filter (53) receiving the horizontal synchronization signal (S_{HS}) and providing the latch control signal (S_{LC}), the latch

control signal (S_{LC}) comprising pulses, each pulse being associated with a parasitic pulse (40).